

**ABSTRACT**

A shift register includes stages shifting an input signal with phase-delayed control signals and first and second supply voltages, and for applying shifted input signals as output signals and as input signals of succeeding stages. Each of the stages includes a first controller selectively applying an input signal and a first supply voltage to a first node between first to third transistors; a second controller selectively applying the first and second supply voltages to a second node between fourth and fifth transistors; and an output buffer selectively applying a predetermined control signal and the first supply voltage as an output signal to a stage output line between sixth and seventh transistors, wherein the fifth transistor may be turned on to sustain a voltage present at the second node equal to the first supply voltage when the fourth transistor is turned off.